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LPC24XX external memory bus example

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Document information

Info	Content
Keywords	LPC24XX, EMC, memory, SDRAM, SRAM, flash
Abstract	This application note will detail an example design illustrating how to connect asynchronous and dynamic memory elements to the external memory bus of the LPC24XX. This note also includes a set of suggested design rules which apply to both the schematic capture and layout phases of PCB design.

Revision history

Rev	Date	Description
1	20100706	Initial version

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1. Introduction

The LPC24XX provides multiple static and dynamic memory chip select outputs to enable designers to work with a large set of memory topologies. Designers must take care to ensure that their PCB satisfies the electrical and timing characteristics of the external memory bus or their embedded systems may not be able to operate reliably at maximum frequency. Consult with the “Dynamic characteristics: Dynamic external memory interface” and “Dynamic characteristics: Static external memory interface” sections of the LPC24XX Data Sheet for a detailed list of specifications.

The ability of a memory bus with multiple devices to operate properly is dependent on several factors: the electrical characteristics of the memory devices, the operating frequency of memory transactions, the length of the traces between the LPC24XX and memory device, as well as the voltage levels being used.

2. Suggestions for achieving peak performance

Several factors can affect the performance of an embedded system using the LPC24XX. Signal integrity of the external memory bus is important in order to achieve robust operation at 72 MHz. Operating performance can also be negatively impacted by the choice of memory topologies in a design.

One may need to evaluate whether a single or dual memory device design is preferred. In order to reduce the size of a PCB, a designer may choose to use a single 16-bit memory device in their system. This would meet the loading requirements on the external memory bus and may operate reliably at 72 MHz, but because the data bus is constricted performance will be degraded.

In order to improve the performance, one might simply add an additional 16-bit memory. Without proper consideration to signal integrity, however, this additional 16-bit device may result in a marginal design. If care is not taken to properly fan out the memory bus to all memory elements, the bus may become improperly loaded. This can be mitigated by using buffer circuitry in the case of static memories, but the additional parts can increase board costs. In the case of dynamic memories this can be overcome by using a lower clock frequency, at the price of reducing performance.

As seen in Table 1, if a design used an AM29LV64 flash memory and a combination of two 16-bit HYB39S128 SDRAM, the I/O pins would have a loading of 18.0 pF (without taking parasitic capacitances of the PCB into account). This may appear to have a large safety margin when compared to the LPC24XX’s maximum rating of 30.0 pF. Many designs are not this simplistic, however, and if the design required the use of an additional SRAM (or a peripheral device using an SRAM interface) the loading on the data bus could increase beyond the rated limit.

The recommended topology consists of a single 32-bit wide SDRAM memory device. This way the bus loading is not excessive, nor are additional data transfers required to achieve maximum throughput.

Always remember to properly configure the EMC in software to match the memory topology for a given design. Each channel’s EMCDynamicConfig register should be configured as per Table 87 of the LPC24XX User Manual to ensure proper functionality. Also note that the EMC of the LPC24XX supports a maximum of 256 MB per memory range.

Table 1. Loading characteristics

Maximum loading by various memory ICs

Part	Clock pin	Data width	Native input, 32 bit wide input	Input/output
HYB39S128	3.5 pF	16 bits	3.8 pF , 7.6 pF	6.0 pF
MT48LC4M32B2	4.0 pF	32 bits	4.0 pF , 4.0 pF	6.5 pF
M29EW	n/a	16 bits	7.0 pF , 14.0 pF	5.0 pF
AM29LV64	n/a	16 bits	7.5 pF , 15.0 pF	12.0 pF
CY62256VN	n/a	8 bits	6.0 pF , 24.0 pF	8.0 pF

3. Suggested design rules

The following rules act as a collection of guidelines, which if properly followed will reduce the risk of a design failing. However, in some instances it is not possible to meet all of these requirements; if proper signal integrity analysis of the design is conducted, depending on the results of simulation it may be possible to build a robust design which does not utilize every one of these recommendations.

3.1 General rules

Because Dynamic memories rely heavily on their clocks, it is important to minimize latency and jitter on the clock output signals in relation to the rest of the external memory bus. A six layer PCB with power planes is recommended for high performance designs. Ensure that both the LPC24XX and all memory elements are properly decoupled from their power supplies with low-ESR capacitors (MLCC or Tantalum). Consult all chosen memory device documentation for recommended decoupling capacitors arrangements. If analysis cannot be done, a general recommendation of at least a single 4.7 uF bulk capacitor per device in combination with a 100 nF per supply pin should work reliably in most cases.

When using a mixture of dynamic and static memories (as shown in the following example) it is recommended that all signals being used in the static memory bus are buffered prior to arriving at memory devices. Any signals which arrive at a connector or are taken off board should also be buffered. It is recommended that the entire bus, including all control and address signals (rather than simply the data lines) be buffered to ensure all signals arrive downstream with minimal jitter or skew.

Dynamic memories typically are not buffered due to their synchronous nature. Ensure that the selected memory devices do not exceed the electrical characteristics of the CLKOUT signals. In order to reduce reflections on the dynamic memory bus, it is recommended that the data bus on the LPC24XX and on all dynamic memory devices is properly terminated.

3.2 Schematic

When using multiple banks of dynamic memory, evenly distribute CLKOUT[1:0] amongst the memory banks, rather than disproportionately loading any individual clock. Be sure that the connectivity of BA[1:0] on memory devices is connected to their multi-function pins A[14:13] on the LPC24XX (even when using lower density memories with fewer address lines).

3.3 Placement

Memory elements should be placed as close as possible to the LPC24XX. If interconnecting of the memory bus cannot be accomplished without the use of vias, care should be taken to ensure that no unnecessary vias are added to the traces. While it is not a strict requirement, stripline transmission lines are preferred.

3.4 Routing

Non-buffered interconnecting traces should be as short as possible, and are not recommended to exceed 50 mm. When a bus is branched, ensure that all stub connection lengths are within ±5.0 mm of each other. Orthogonal connections should jog using 45° tapers or smooth curves, rather than 90° corners. See Fig 9 for the recommended physical placement of devices.

4. Example: Embedded uCLinux (no-MMU support)

A common use for the LPC24XX involves the device running an embedded distribution of the Linux operating system without MMU support, such as uCLinux. Typically these designs will use a non-volatile memory (such as parallel NOR flash) to store the root file system and a compressed kernel image, which is copied by the boot loader into a high speed memory (such as an SDRAM) for execution. This application note will cover the design and analysis of a simple embedded system using an LPC24XX with NOR flash and SDRAM while insuring that it will operate at maximum frequency.

The non-volatile memory is usually accessed only during system startup by the boot loader and during field updates. Because of this limited use a designer will typically accept the tradeoff between the performance penalty incurred by the use of a 16-bit wide device and reduced cost due to decreased part count.

5. Design details

The design in this application note is as follows: A single 32-bit wide SDRAM will be connected to the external memory controller without the use of external buffering circuitry. It is critical that the memory be connected with traces which do not add excessive capacitance to the bus. A thorough design analysis should always be conducted to ensure that the electrical specifications of the LPC24XX are met.

The LPC24XX will boot from a single 16-bit wide NOR FLASH memory with buffered data, address and control signals. This example design is meant primarily to illustrate how to buffer the asynchronous bus of the LPC24XX, and it is assumed that a real end user design may require additional asynchronous memory devices in addition to the NOR FLASH. Notice that the memory structure of the MT48LC4M32B2 is compatible with the “32 bit external bus high-performance address mapping” of the EMC as seen in Table 87 in the LPC24XX User Manual. Also note that the MT48LC4M32B2 can only operate at frequencies above 50 MHz with CAS latencies of 2 or 3.

When using LPC2420/60/70 parts care must be taken to ensure boot memory is connected to the proper chip select lines and that the BOOT[1:0] pins properly reflect the bus width of the attached memory when they are sampled at startup. Section 8.6 “LPC2420/60/70 boot control” of the LPC24XX User Manual details the startup behavior and requirements.

6. Example IC bill of materials

Table 2. Bill of materials

Designator	Manufacturer	Part Number	Description
U1	NXP	LPC2478FBD208	ARM7 32-bit microcontroller
U2	Micron	MT48LC4M32B2	SDRAM 128 Mbit
U3,U4,U5	NXP	74ABT162245A	16-bit bus transceiver
U6	Spansion	AM29LV641DH101REI	4M x 16 flash memory
C1-C12,C14-C17,C19-C22,C24-C27,C29-C32	Murata	GRM155R61A104KA01D	0.100 uF 25V X7R 0603
C13,C18,C23,C28	Kemet	C0603C475K8PACTU	4.7 uF 10V X5R 0603
R11-R12	Unspecified	Generic 0 Ohm	Debug jumper
R5,R7,R13-R16	Unspecified	Generic 500-1500 Ohm	Pull up/down
R1-4,R6,R8-R10	CTS	742C163220JPTR	20.0 Ohm array

7. Schematics

Please be aware that the following schematics are lacking many application specific connections, such as input power conversion, USB connectivity, additional LPC24XX peripherals, etc. While care has been taken to demonstrate a full performance example using the external memory bus, the included schematics alone are not sufficient for PCB fabrication.

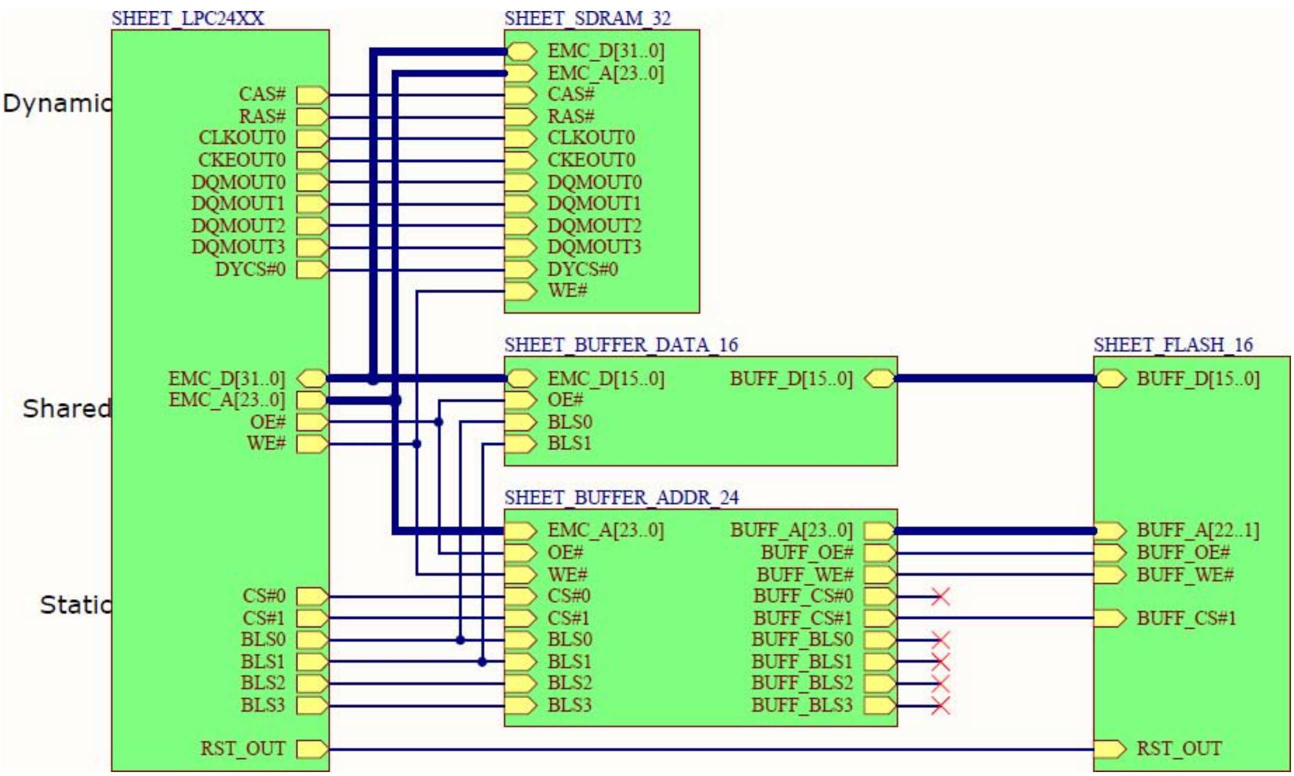

Fig 1. Simplified block diagram

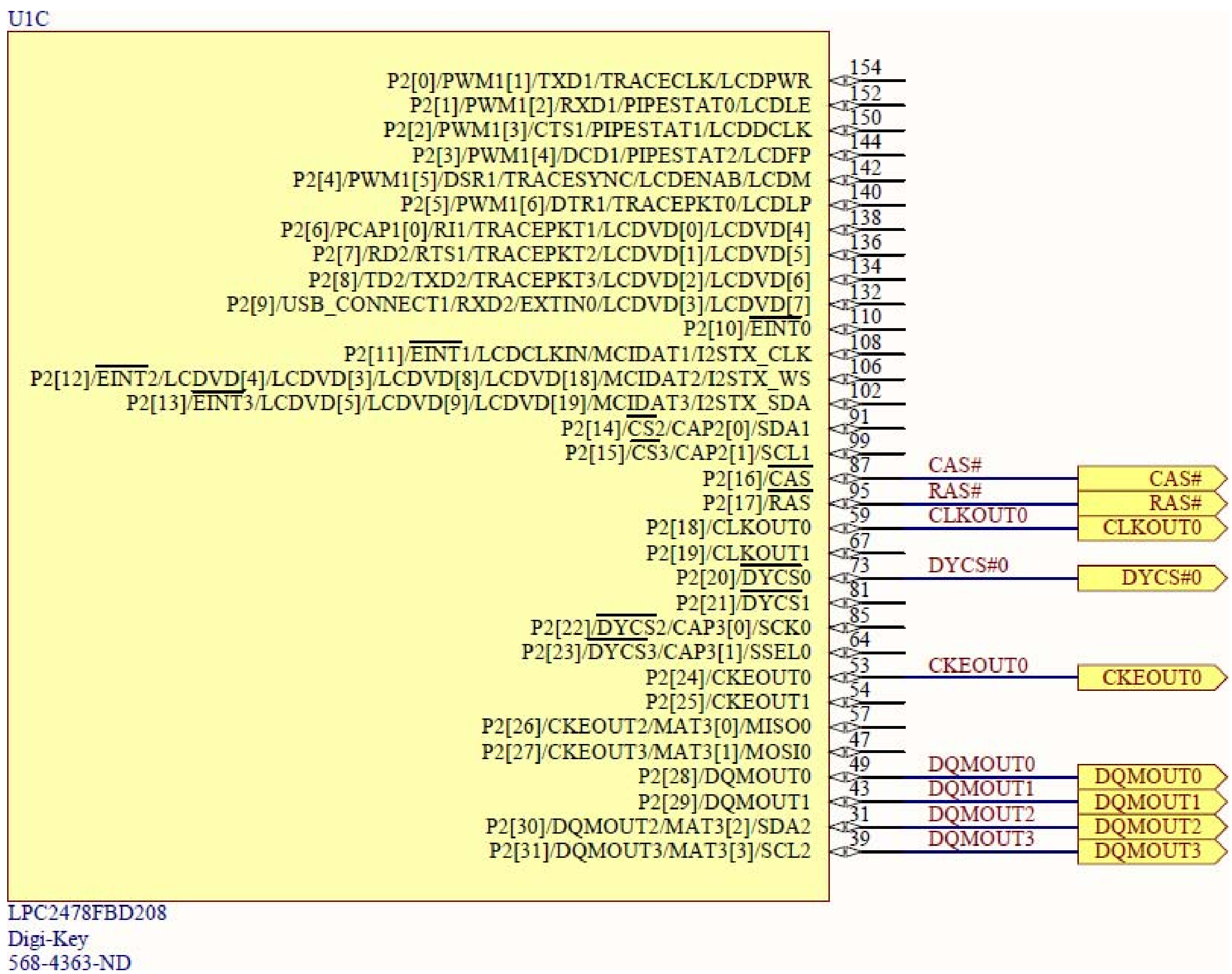

Fig 2. LPC24XX external memory controller interface: control signals

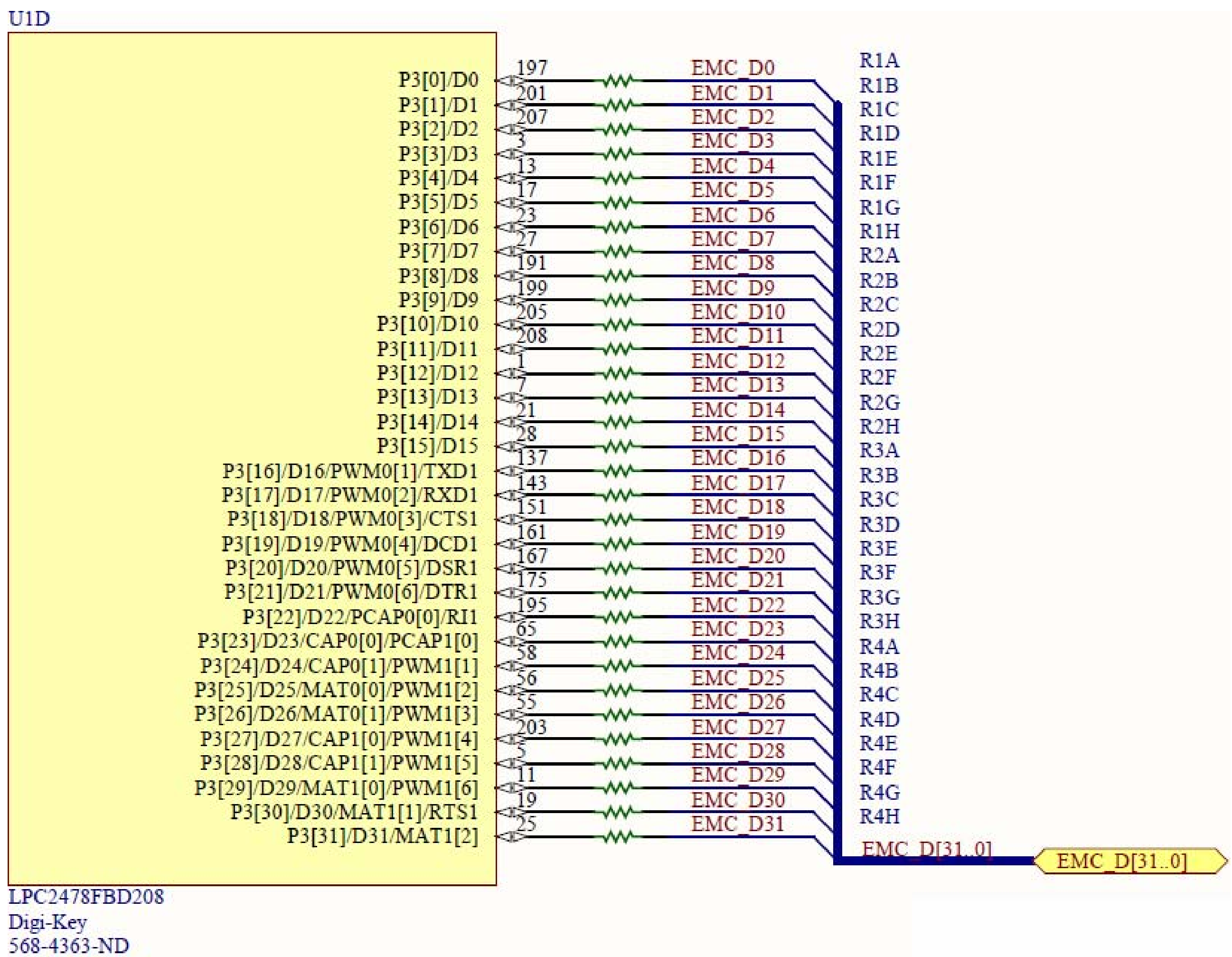

Fig 3. LPC24XX external memory controller interface: data signals

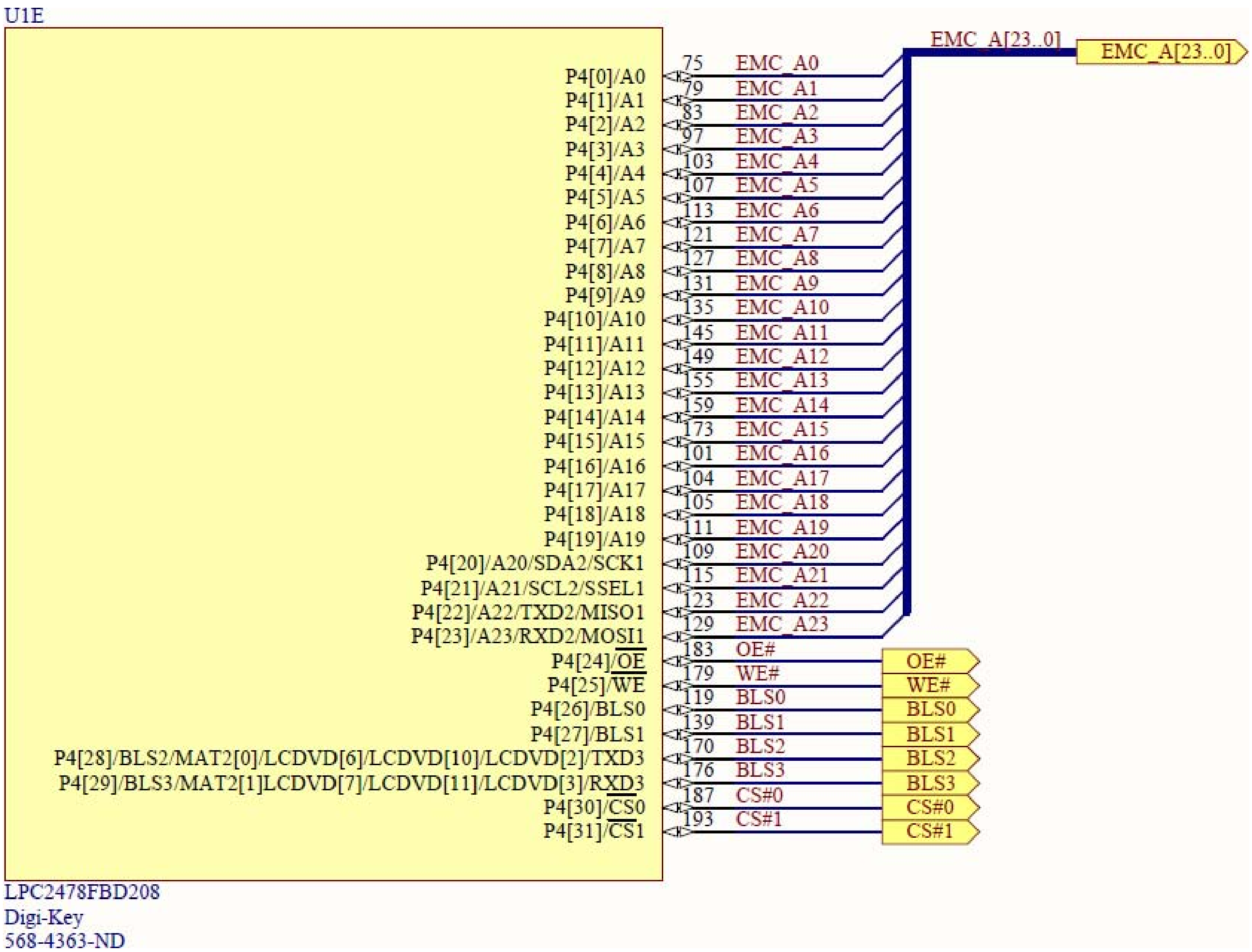

Fig 4. LPC24XX external memory controller interface: address, control signals

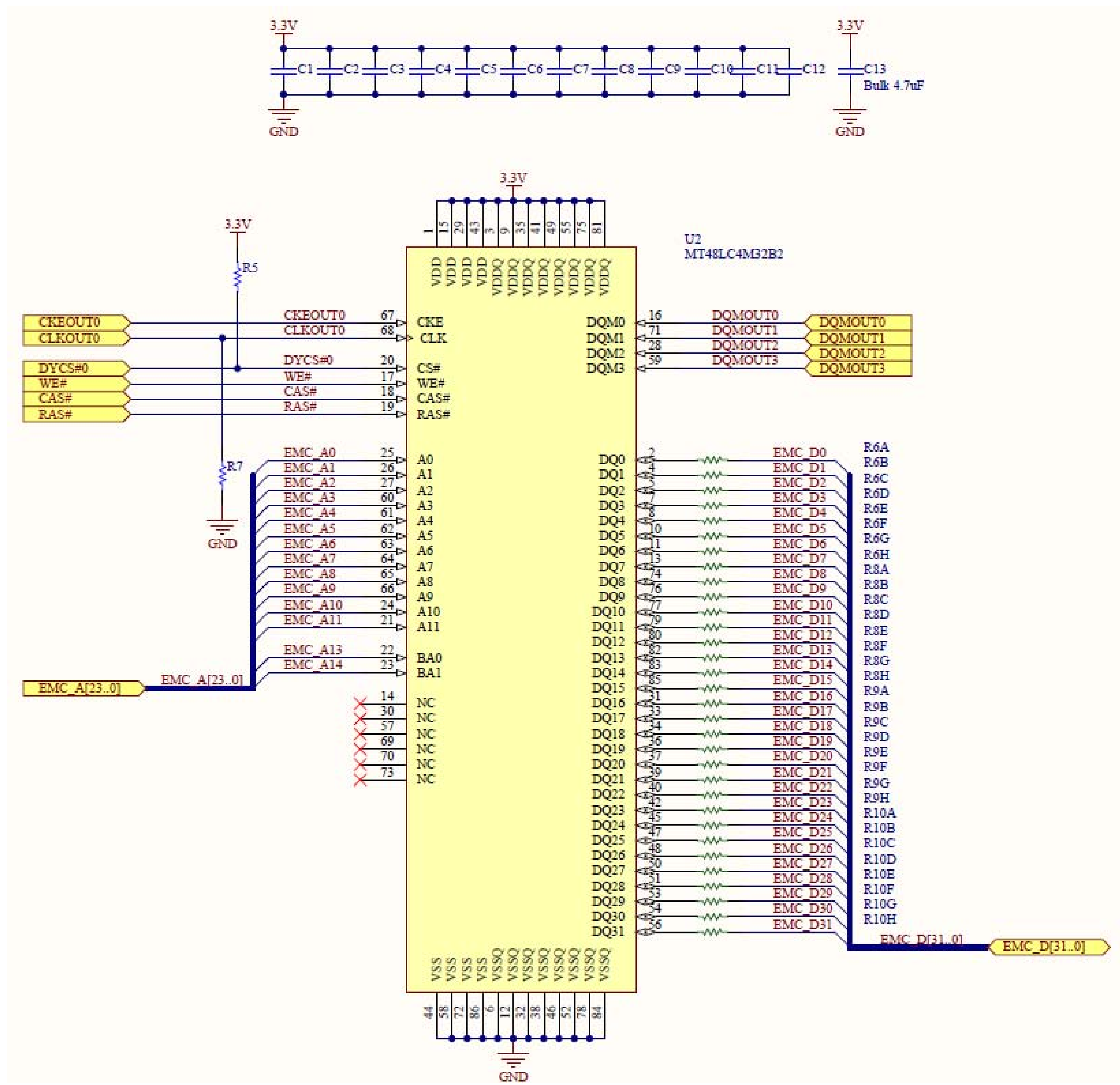

Fig 5. SDRAM interface

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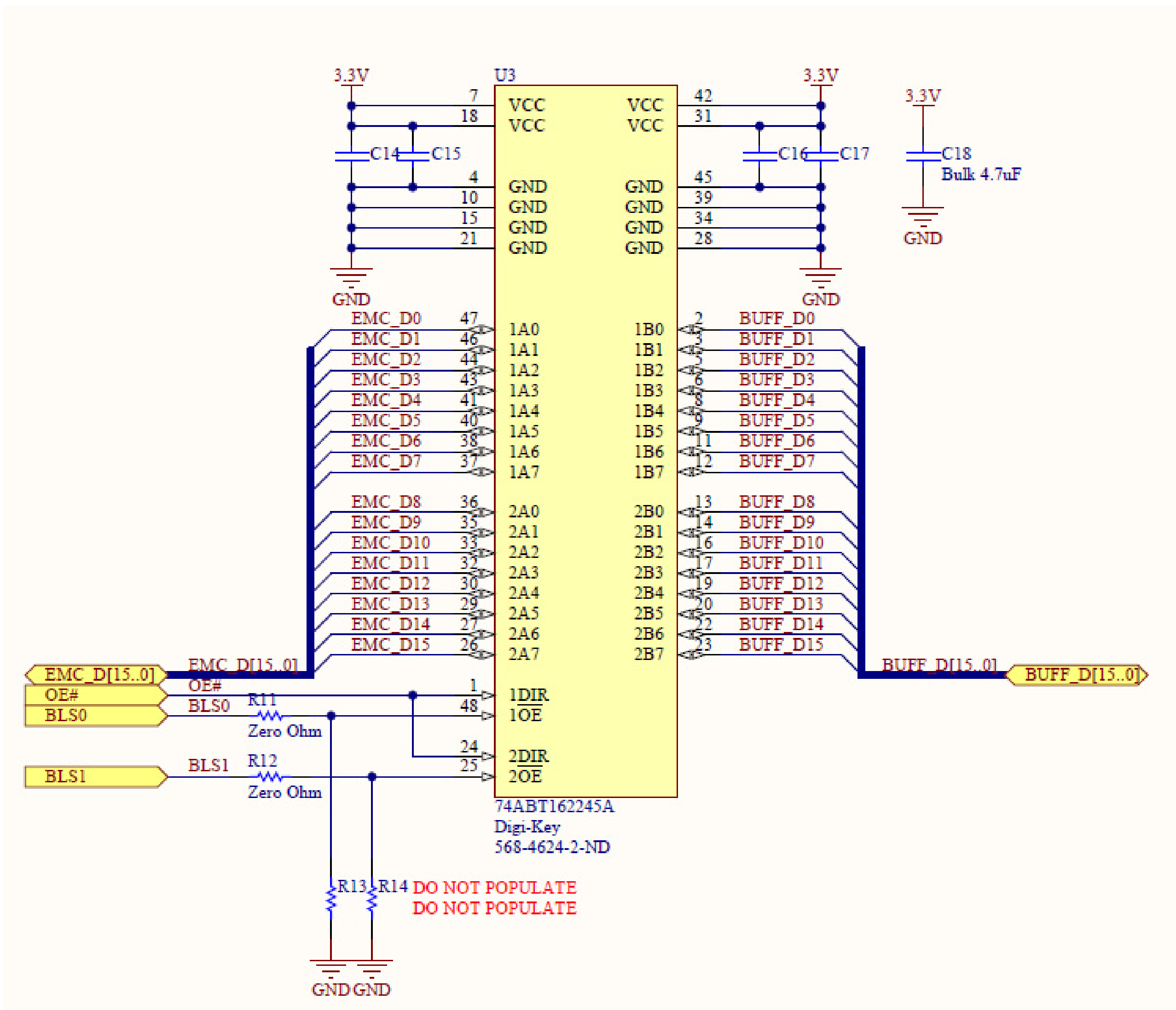

Fig 6. Data[15:0] buffering, BLS[1:0] control output enable

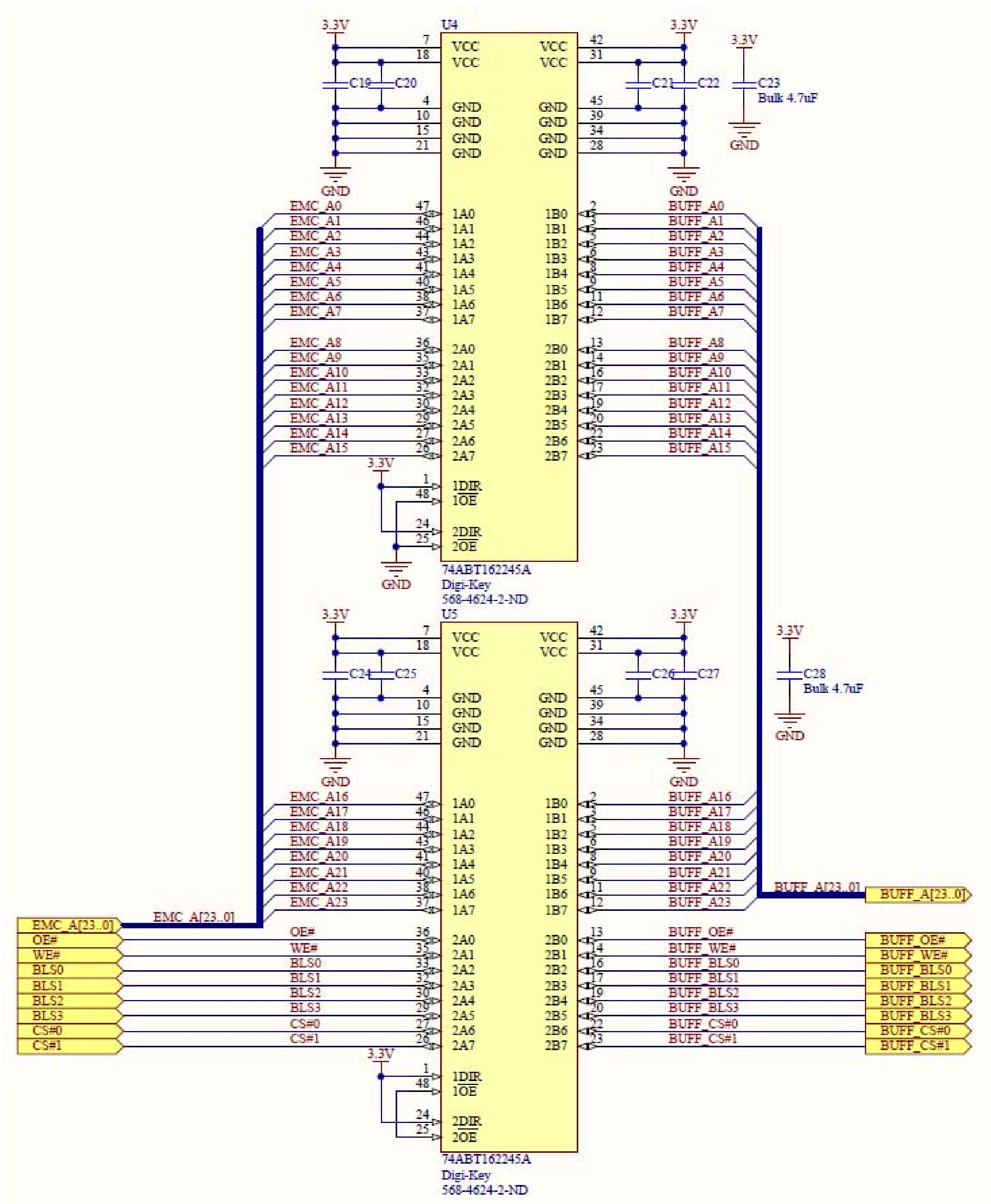

Fig 7. Address[23:0] buffering, static control buffering

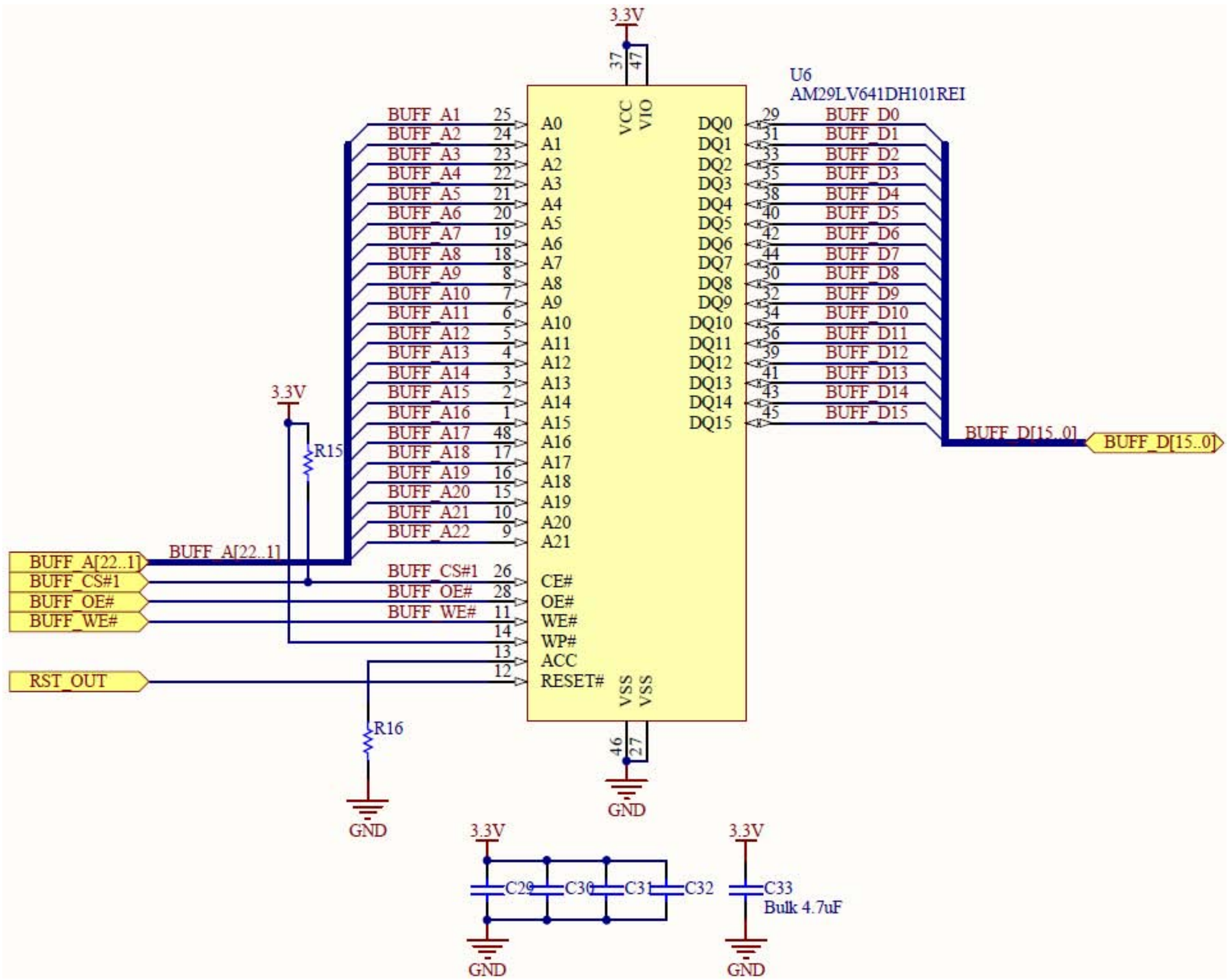

Fig 8. NOR flash memory, CS#1 is primary boot memory source

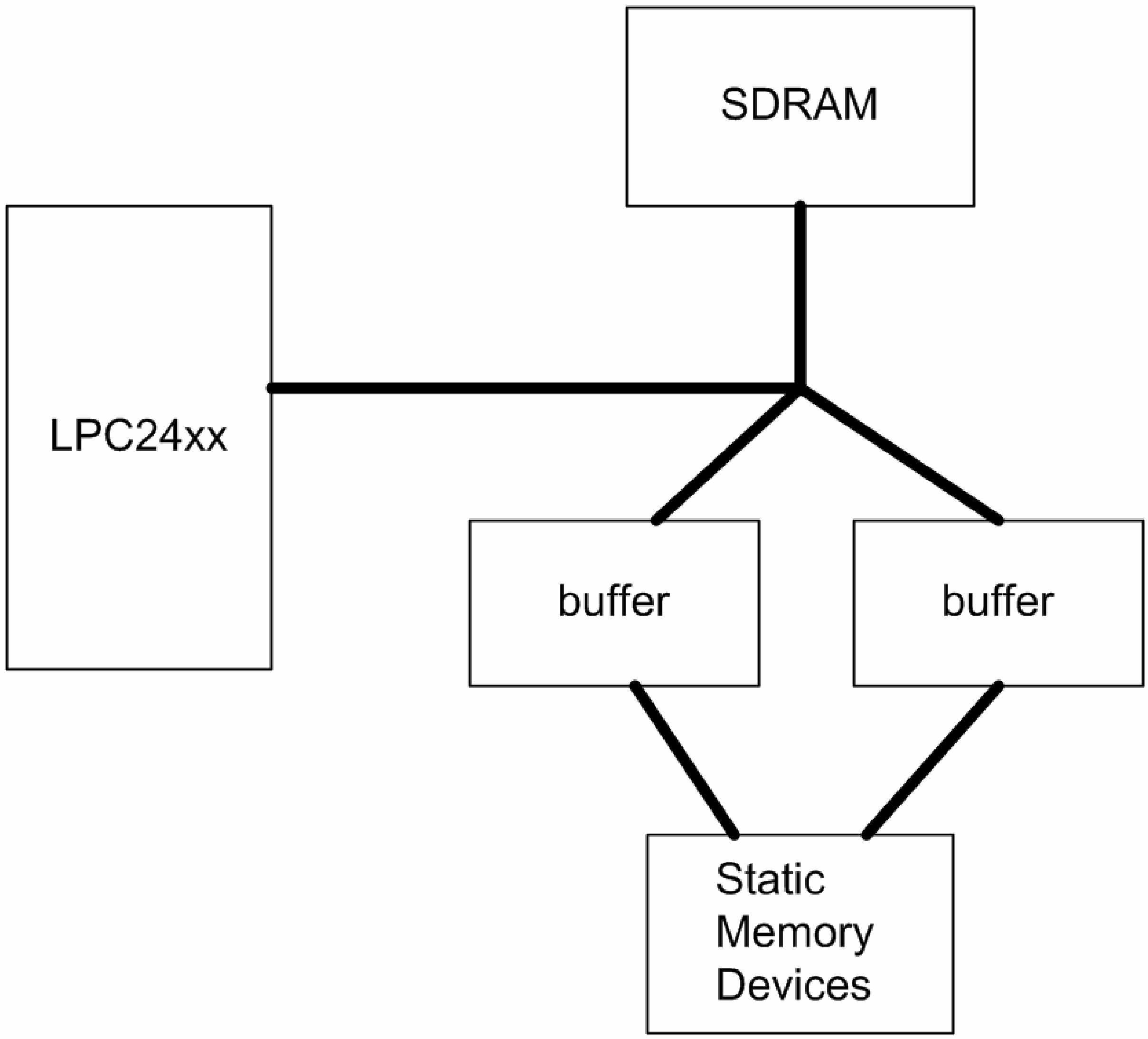

Fig 9. Recommended physical placement

8. Conclusion

This example project should illustrate how to properly design a PCB making use of the LPC24XX's external memory bus. Be aware that the design in this application note is relatively simplistic, and more complicated designs will warrant thorough design analysis, with a focus on signal integrity.

Always take care to carefully read the data sheets for all devices on the memory bus, including the LPC24XX's electrical and timing specifications.

By following the design rules included in the application note, designers can avoid many common (and easily corrected) pitfalls which might have otherwise prevented their systems from operating at the maximum system speed.

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